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PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10074309	02/11/2002	365	194	~~2818~~ 2824	404

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**CONTINUING DATA VERIFIED:

NONE

** FOREIGN APPLICATIONS VERIFIED:

REPUBLIC OF KOREA 2001-8141 02/19/2001

PG-PUB DO NOT PUBLISH ☐ RESCIND ☐

Foreign priority claimed ☑ yes ☐ no

35 USC 119 conditions met ☑ yes ☐ no

Verified and Acknowledged Examiners's intials

ATTORNEY DOCKET NO 5649-944

TITLE : Integrated circuit devices having delay circuits for controlling setup/delay times of data signals that are provided to memory devices and methods of operating same

U.S DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G
ISSUE FEE: Amount Due / Date Paid	Primary Examiner	DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAMER	PREPARED FOR ISSUE	Application Examiner

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